苏州大学实验报告

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| 课程名称 | | 模拟与数字电路设计 | | | | | | | 成绩 |  |
| 指导教师 | | 屈蕴茜 | | 同组实验者 | | 无 | | 实验日期 | 2022.11.9 | |

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| 实 验 名 称 | 实验五 计数器实验 |

1. 实验目的

1.掌握74LS161型集成计数器的使用

1. 实验设备
   1. TD-DS+/TD-DS实验箱一台
   2. 74LS161同步4位二进制计数器一片
   3. 74LS00 2输入端四与非门一片
2. 实验内容

1. 74LS161功能测试

2. 用74LS161和门电路设计实现一个十进制计数器

1. 实验原理

**同步4位二进制计数器74LS161**

74LS161为同步4位二进制计数器，其引脚及逻辑符号如图1-1所示，其功能表如表1-1所示。



图1-1 74LS161引脚图

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | | **D3D2D1D0** | **CLK** | **CLR** | **EP** | **ET** | **LOAD** | **功能** | **Q3Q2Q1Q0** | **Co** | | 0110 | × | 0 | × | × | × | 清零 | 0000 | 0 | | 0110 | ↑ | 1 | × | × | 0 | 接数 | 0110 | 0 | | 0110 | ↑ | 1 | 1 | 1 | 1 | 计数加1 | 0111 | 0 | | 0110 | × | 1 | 1 | 0 | 1 | 保持 | 0000 | 0 | | 0110 | × | 1 | 0 | 1 | 1 | 保持 | 0000 | 0 | | 0110 | × | 1 | 0 | 0 | 1 | 保持 | 0000 | 0 | |
| 表1-1 74LS161功能表 |

1. 实验步骤与结果
   1. **74LS161功能测试**

按图接线，输入端接到逻辑电平开关上，时钟输入端接单次脉冲，输出端接逻辑电平显示，根据图2-1连接线路，完成芯片功能测试，验证表2-1。



图2-1 74LS161功能测试

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | | **D3D2D1D0** | **CLK** | **CLR** | **EP** | **ET** | **LOAD** | **功能** | **Q3Q2Q1Q0** | | 0110 | × | 0 | × | × | × | 清零 | 0000 | | 0110 | ↑ | 1 | × | × | 0 | 接数 | 0110 | | 0110 | ↑ | 1 | 1 | 1 | 1 | 计数加1 | 0111 | | 0110 | × | 1 | 1 | 0 | 1 | 保持 | 0000 | | 0110 | × | 1 | 0 | 1 | 1 | 保持 | 0000 | | 0110 | × | 1 | 0 | 0 | 1 | 保持 | 0000 | |
| 表2-1 74LS161功能表 |

**2. 用74LS161和门电路设计实现一个十进制计数器。**

令CLR=EP=ET=LOAD=1，D3D2D1D0的初始值为0000，十进制计数器的合法状态表如表3-1所示。

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| |  |  |  | | --- | --- | --- | | **计数顺序** | **Q3Q2Q1Q1** | **CLR** | | 0 | 0000 | 1 | | 1 | 0001 | 1 | | 2 | 0010 | 1 | | 3 | 0011 | 1 | | 4 | 0100 | 1 | | 5 | 0101 | 1 | | 6 | 0110 | 1 | | 7 | 0111 | 1 | | 8 | 1000 | 1 | | 9 | 1001 | 1 | |
| 表3-1 十进制计数器状态表 |

画出卡诺图并化简逻辑函数为与非表达式得



修改逻辑电路图为



并验证功能表。

1. 实验总结

通过此次实验，我对数字电路有了更深入的了解。掌握了74LS161型集成计数器的使用。设计了十进制的计数器电路。实验总体来说较为顺利。